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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,974	02/09/2004	Adnan Khaleel	NWISP049	2184

22434 7590 09/23/2005

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,974	KHALEEL, ADNAN	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33 and 35-46* is/are rejected.

7)☒ Claim(s) *34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-33 and 35-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilson (U.S. Patent Application Publication 2002/0049824).

Regarding claim 1:

Wilson discloses a computer system comprising a processor and a memory (fig. 1, unit 102, 100, 202, 204) , the processor being operable to initiate transactions involving the memory (fig. 1, unit 20, 302), the computer system further comprising a latency counter operable to generate a latency count for each of selected ones of the transactions (page 2, section 0029), and a plurality of histogram counters (page 3, section 0044), each histogram counter being operable to count selected ones of the latency counts corresponding to an associated latency range (page 2, section 0029, page 3, section 0044).

Regarding claim 22:

Wilson discloses an interconnection controller for use in a computer system having a plurality of processor clusters (fig.1, unit 102, 202, 302), each cluster including a plurality of local nodes and an instance of the interconnection controller interconnected by a local point-to-point architecture (fig. 1, unit 20), the

interconnection controller being operable to process transactions associated with the computer system, the interconnection controller further comprising a latency counter operable to generate a latency count for each of selected ones of the transactions, and a plurality of histogram counters, each histogram counter being operable to count selected ones of the latency counts corresponding to an associated latency range (page 2, section 0029, page 3, section 0044).

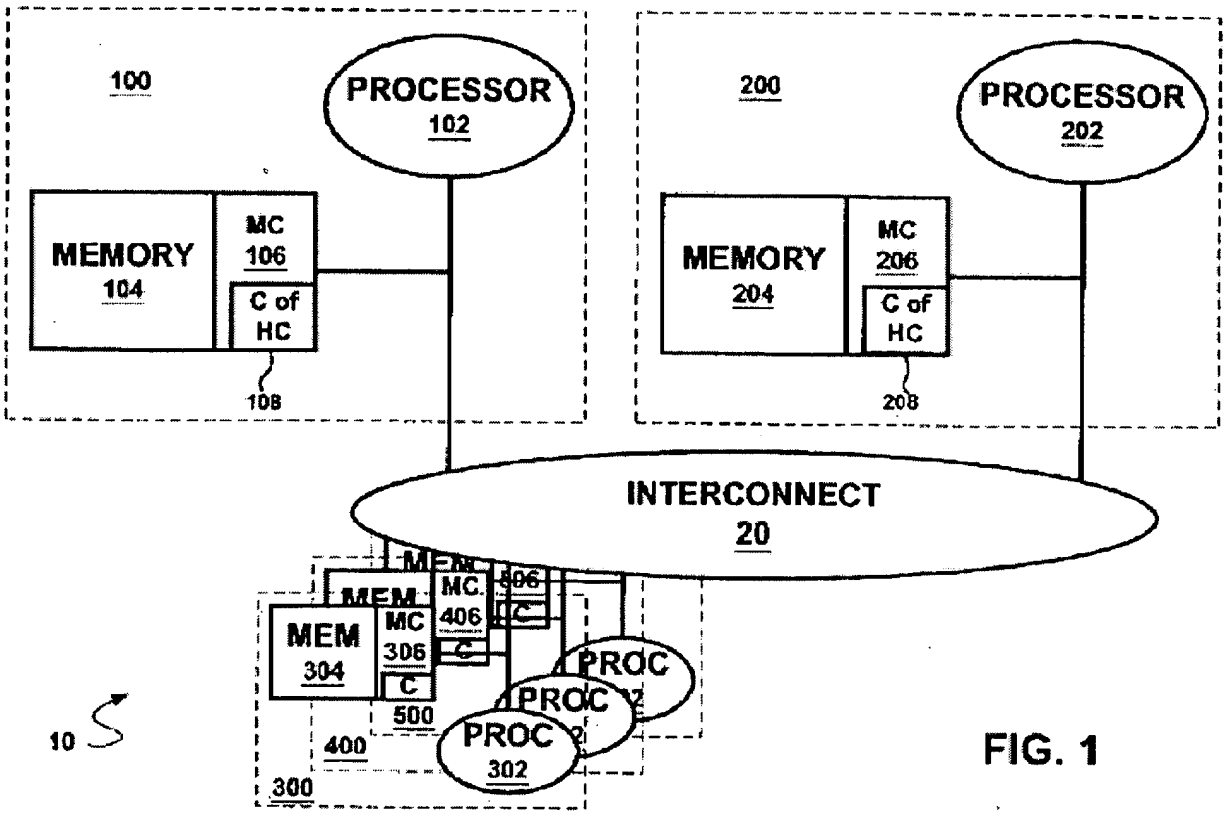

FIG. 1

Regarding claim 38:

Wilson discloses a computer-implemented method for measuring performance of a computer system, comprising: generating a latency count for each of a plurality of transactions in the computer system (fig. 1, unit 300, 100, 200, page 2, section

0029, page 3, section 0044), and counting selected ones of the latency counts corresponding to each of a plurality of latency ranges, thereby generating latency distribution data (page 2, section 0029, page 3, section 0044).

Regarding claim 41:

Wilson discloses an electronic system characterized by a plurality of transactions, the electronic system comprising a latency counter operable to generate a latency count for each of selected ones of the transactions (page 2, section 0029, page 3, section 0044), and a plurality of histogram counters, each histogram counter being operable to count selected ones of the latency counts corresponding to an associated latency range (page 2, section 0029, page 3, section 0044).

Regarding claims 2, 23, Wilson discloses each histogram is programmable (fig. 3, unit 110-122); Regarding claim 3, Wilson discloses beginner value (fig. 3, unit 110, 112, 114); Regarding claims 4, 25, Wilson discloses the latency counter is operable to count clock cycles between a first event and a second event associated with each of the selected transactions, the latency count for each of the selected transactions corresponding to a number of clock cycles (page 3, section 0044, fig. 3, unit 114, fig. 1, unit 102); Regarding claim 5, Wilson discloses first and second events is programmable (fig. 3, unit 110-122); Regarding Claim 6, Wilson discloses generating transaction type ((fig. 1, unit 300, 400, 500); Regarding claim 7, Wilson discloses the latency counter is one of plurality of latency counters, each latency counter being operable to generate the

latency count for a portion of the selected transactions (fig. 2, unit 110-122); Regarding claims 8, 27, Wilson discloses the latency counter and the histogram counters are operable to generate and count the latency counts at run-time (fig. 2, unit 110-122, 252-270); Regarding claims 9, 28, Wilson discloses the processor is operable to alter a run-time parameter in response to latency information derived from the histogram counters (page 2, section 0029, page 3, section 0044); Regarding claim 10, Wilson discloses the processor is one of a plurality of processors operable to initiate the transactions (fig. 1, unit 300, 102, 202); Regarding claim 11, Wilson discloses the processors and memory are interconnected with a point-to-point architecture (fig. 1, unit 300, 400, 102, 202); Regarding claim 12, Wilson discloses the processors and memory are interconnected with a shared-bus architecture (page 2, section 0023); Regarding claim 13, Wilson discloses the processors are configured in a plurality of processor clusters, each cluster including a plurality of local nodes and an interconnection controller interconnected by a local point-to-point architecture, the interconnection controllers being operable to facilitate interaction among the clusters, and

wherein the latency and histogram counters are implemented in each of the interconnection controllers (fig. 1, unit 102, 104, 108, 106, 202, 204, 206, 208, page 2, section 0023-0030); Regarding claim 14, Wilson discloses the interconnection controller in each cluster comprises a plurality of protocol engines for processing the transactions, and wherein at least one of the

interconnection controller and the local nodes in each cluster is operable to map the transactions to the protocol engines according to destination information associated with the transactions, and wherein the latency and histogram controllers are implemented in each of the protocol engines (fig. 1, unit 102, 104, 108, 106, 202, 204, 206, 208, page 2, section 0023-0030).

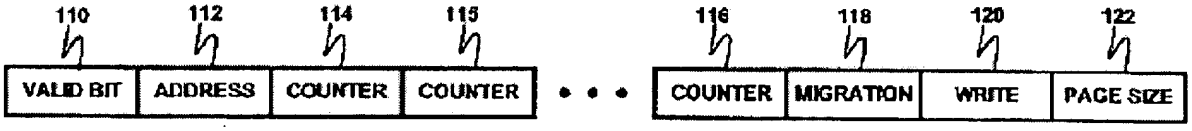

FIG. 2

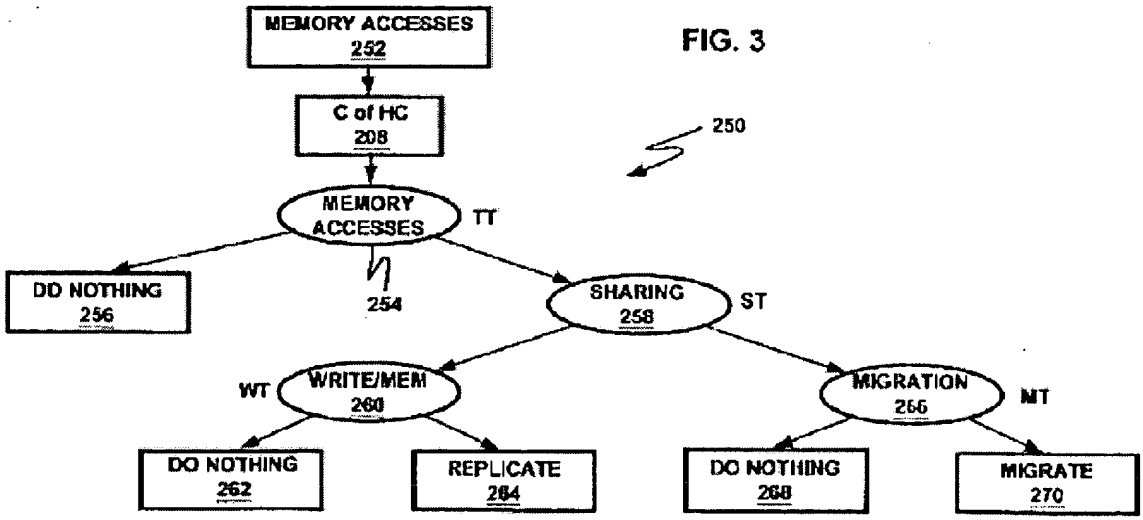

FIG. 3

Regarding claim 15, Wilson discloses the plurality of protocol engines in each interconnection controller comprises at least one remote protocol engine for processing first ones of the transactions targeting remote memory, and at least one local protocol engine for processing second ones of the transactions

targeting local memory (fig. 1, unit 100, 300, 20, page 2, section 0023-0029); Regarding claim 16, Wilson discloses the plurality of protocol engines in each interconnection controller comprises at least one remote protocol engine for processing first ones of the transactions targeting remote memory, and at least one local protocol engine for processing second ones of the transactions targeting local memory (fig. 1, unit 104, 106, 108, 304, 302); Regarding claim 17, Wilson discloses the interconnection controllers are further operable to facilitate cache coherency across the computer system (fig. 1, unit 304, 204, 104, 20); Regarding claim 18, Wilson discloses, an input/output (I/0) device, wherein the processor is further operable to generate second transactions involving the I/0 device, and wherein the latency counter is further operable to generate second latency counts for selected ones of the second transactions, and wherein the plurality of histogram counters are each operable to count selected ones of the second latency counts corresponding to the associated latency range (page 2, section 0023-0030, fig. 3, unit 110-122, fig. 1, unit 100, 200); Regarding claim 19, Wilson discloses based on clock cycles (page 2, section 0027-0030); Regarding claim 20, Wilson discloses events are programmable (fig. 1, unit 100, 200); Regarding claim 21, Wilson discloses transaction type (fig. 1, unit 302, 402, 502);); Regarding claim 24, Wilson discloses each of the latency ranges is part of a window, a beginning value of the window being programmable (fig. 2, unit 110-122); Regarding claim 26, Wilson discloses the latency counter is one

of a plurality of latency counters (fig. 3, unit 115, 116), each latency counter being operable to generate the latency count for a portion of the selected transactions (fig. 2, unit 110); Regarding claim 29, Wilson discloses the latency counter is one of a plurality of latency counters, each latency counter being operable to generate the latency count for a portion of the selected transactions (fig. 2, unit 112, 115); Regarding claim 30, Wilson discloses interconnect controller (fig. 1, unit 20, 102, 202); Regarding claim 31, Wilson discloses an application specific IC (fig. 1, unit 102, 103); Regarding claim 32, Wilson discloses data structure stored therin representative of interconnect controller (fig. 2, unit 110-122); Regarding claim 33, Wilson discloses simulatable representation (fig. 2, unit 110-122); Regarding claim 35, Wilson discloses code description (fig. 2, unit 110-122); Regarding claim 39, Wilson discloses altering a run-time parameter (page 3, section 0041-0044); Regarding claim 40, Wilson discloses related to placement algorithm (page 2, section 0027-0029, fig. 3, unit 110-122); Regarding claims 42, 45, Wilson discloses counter is programmable (page 2, section 0028); Regarding claim 43, Wilson discloses beginning of a value (fig. 3, unit 110); Regarding claim 44, Wilson discloses associated first and second events (page 2, section 0029); Regarding claim 46, Wilson discloses the plurality of histogram counters are operable together to generate latency distribution data, the electronic system further comprising a processor which is operable to dynamically alter a run-time parameter of the electronic system in response to the latency distribution data (page 2, section 0026-0029, page 3,

section 0041-44), Regarding claim 36, Wilson discloses, the code description corresponds to a hardware description language (page 1, section 0011, fig. 3, unit 110-122, fig. 1, unit 102); Regarding claim 37, Wilson discloses, at least masks portion of the interconnect controller (fig. 2, unit 110-122).

Allowable Subject Matter

2. Claim 34 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to teach regarding claim 34, the simulated representation is a netlist.
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments filed 09/12/2005 have been fully considered but they are not persuasive.

A. Applicant argues in the arguments that the prior art does not show the 'opearable to count selected one of the latency counts corresponding to an associated latency range', and the applicant cited the specific teaching of page

32, line 20- page 33, line 21, and fig. 14 of the specification to support the argument.

Wilson discloses 'opearable to count selected one of the latency counts corresponding to an associated latency range' in page 2, section 0026-0029, page 3, section 0043-0046, Wilson uses history counter to access memory so that less paging it is, the faster the system is for memory access and can reach optimum level (page 3, section 0043-0046), Wilson talks about this concept of history reflects latency in the system and is recognize one ordinary skill in the art (page 2, section 0026). As regard to the applicant specific reference on page 32, line 20- page 33, line 21, and fig. 14, the examiner reminds to the applicants that while the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). During patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is

justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

MICHAEL NGHIEM
PRIMARY EXAMINER